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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/516,713	12/01/2004	Wolfgang Schnitt	DE02 0137 US	6751

24738 7590 05/04/2006

PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
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EXAMINER	
LIU, BENJAMIN T	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 05/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/516,713	SCHNITT ET AL.	
	Examiner	Art Unit	
	Benjamin T. Liu	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/1/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Minhloan Tran
Primary Examiner
Art Unit 2826

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/01/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102(b)

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10 are rejected under 35 U.S.C 102(b) as being anticipated by Adan (5,198,379).

With regard to claim 1, figure 3 of Adan discloses a semiconductor-on-insulator (SOI) device, comprising: at least one isolating layer 1 made of a dielectric material; at least one silicon substrate 1A arranged on said isolating layer 1; at least one component (S, 3A, D) integrated in the silicon substrate 1A, which component (S, 3A, D) has at least one slightly doped zone 3A; as well as at least a first, planar, metallization region 6A arranged between the isolating layer 1 and the component (S, 3A, D), between the isolating layer 1 and the slightly doped zone 3A of the component (S, 3A, D), characterized in that at least a second, in particular planar, metallization region 6B is arranged on the side of the silicon substrate 1A facing away from the isolating layer 1, in the area of the component (S, 3A, D), in the area of the slightly doped zone 3A of the component (S, 3A, D).

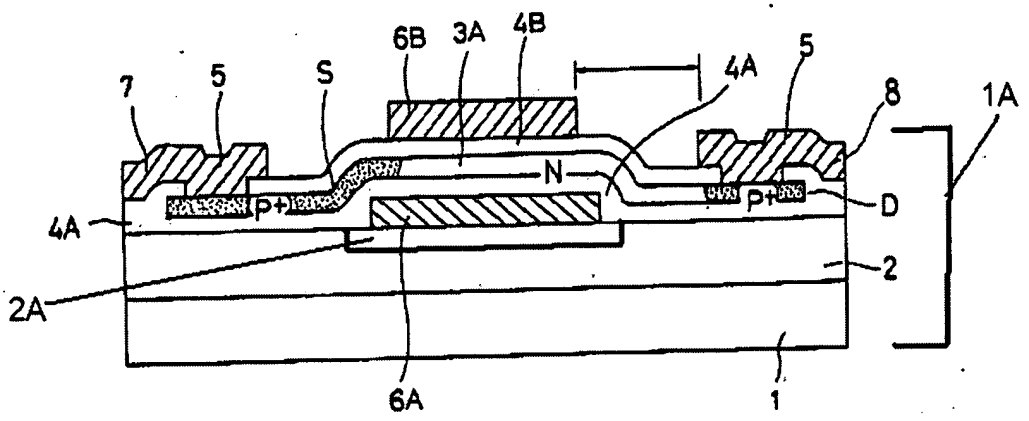

Figure 1: semiconductor device with first passivation layer 2A and silicon substrate 1A

With regard to claim 2, figure 3 of Adan discloses a semiconductor device, characterized in that the silicon substrate 1A comprising the component (S, 3A, D) is fixed onto the isolating layer 1 with at least one fixing medium 2, with an adhesive layer.

With regard to claim 3, figure 3 of Adan discloses a semiconductor device, characterized in that the component (S, 3A, D) is formed by at least one, bipolar, pnp (S, 3A, D) transistor; and the slightly doped zone 3A of the component (S, 3A, D) is formed by the n-doped region of the pnp- transistor.

With regard to claim 4, figure 3 of Adan discloses a semiconductor device, characterized in that the first metallization region 6A is embedded in at least a first, oxide-based, passivation layer 2.

With regard to claim 5, figure 3 of Adan discloses a semiconductor device, characterized in that on the side of the component (S, 3A, D) facing the isolating layer 2, at least one oxide layer 4A borders on the component (S, 3A, D) and/or on the first passivation layer 2A.

With regard to claim 6, figure 3 of Adan discloses a semiconductor device, characterized in that between the component (S, 3A, D) and the second metallization region 6B at least a second, oxide-based passivation layer 4B, is arranged.

With regard to claim 7, figure 3 of Adan discloses a method of manufacturing at least one semiconductor device, in particular, wherein: at least one isolating layer 1 made of a dielectric material is provided with at least one silicon substrate 1A using, adhesive means; at least one component (S, 3A, D) having at least one slightly doped zone 3A is integrated in the silicon substrate 1A; and at least a first, in particular planar, metallization region 6A is arranged between the isolating layer 1 and the component (S, 3A, D), in particular between the isolating layer 1 and the slightly doped zone 3A of the component (S, 3A, D), characterized in that at least a second, in particular planar, metallization region 6B is provided on the side of the silicon substrate 1A facing away from the isolating layer a, in the area of the component (S, 3A, D), in the area of the slightly doped zone 3A of the component (S, 3A, D).

With regard to claim 8, figure 3 of Adan discloses a method, characterized in that the first metallization region 6A is embedded in at least a first, oxide-based passivation layer 2A.

With regard to claim 9, figure 3 of Adan discloses a method, characterized in that at least a second, in particular buried, passivation layer 4B, which is in particular oxide-based, is arranged between the component (S, 3A, D) and the second metallization region 6B.

With regard to claim 10, figure 3 of Adan discloses an application of at least a first, planar, metallization region 6A as well as at least a second, planar, metallization region 6B to electrically shield, on both sides, at least a component (S, 3A, D) incorporated in the silicon substrate 1A of a SOI device, to electrically shield, on both sides, at least a slightly doped zone 3A of the component (S, 3A, D).

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin T. Liu whose telephone number is (571) 272-6009. The examiner can normally be reached on Mon-Fri 9:30 AM-6:00AM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BTL
4/6/06